## Capacitance Sensor Operation

This is not intended as a rigorous analysis of the FBV sensor circuit, but should rather be thought of as an explanation of the general mechanism which makes it work.

In this analysis, two things are ignored: the fact that the $\pm 5 \mathrm{~V}$ drive voltage is capacitor coupled, which means that there may be a small common-mode bias to the $\pm 5 \mathrm{~V}$ voltage levels. That is, they may not be exactly equal and opposite. Also it is assumed here that the transfer capacitor C 3 initially is not charged. In fact when operating each cycle will start out with it having a voltage which approximates the circuit output.


During the $8 \mu \mathrm{sec}$ phase 1 of the switching cycle the sensor capacitors Ca and Cb are charged to -5 V and C 3 is not present, being connected at that time to the switch output.

During phase 2, the transfer capacitor C 3 is connected between Ca and Cb and we want to determine what its voltage will be as a result of any imbalance between Ca and Cb .

Mesh 1 and mesh 2 are drawn to represent two closed current-paths in the circuit, noting that each properly defines a closed loop when the power supplies are drawn in. Anyone familiar with electrical circuit theory may recognize that identifying such meshes is the first step in writing the complete matrix equations which define the circuit voltages and currents. For us, the important fact is that for a linear circuit such as ours, the currents in each of the meshes and their effects may be computed individually and the results summed to obtain the overall values.


In mesh 1:
The total capacitance C 1 of Cb in series with C 3 is

$$
\mathrm{C} 1=(\mathrm{C} 3 \mathrm{Cb}) /(\mathrm{C} 3+\mathrm{Cb})
$$

The total charge transferred

$$
\mathrm{Q} 1=\mathrm{C} 1 \mathrm{dV}=(\mathrm{C} 3 \mathrm{Cb}) /(\mathrm{C} 3+\mathrm{Cb}) 10 \mathrm{~V}
$$

Using $\mathrm{Q}=\mathrm{CV}$, we can compute the voltage change, dV 3 , in C 3 as $\mathrm{dV} 3=(\mathrm{C} 1 / \mathrm{C} 3) \mathrm{dV}=(\mathrm{Cb} \mathrm{dV}) /(\mathrm{C} 3+\mathrm{Cb})$

Similarly in mesh 2 :
The total voltage change of C3 is
$\mathrm{dV} 3=-(\mathrm{Ca} \mathrm{dV}) /(\mathrm{C} 3+\mathrm{Ca})$
Summing the results from both mesh computations the net voltage change on C3
$\mathrm{dV} 3=\mathrm{dV}(\mathrm{Cb} /(\mathrm{C} 3+\mathrm{Cb})-\mathrm{Ca} /(\mathrm{C} 3+\mathrm{Ca}))$
And since C 3 is approximately 100 times larger than either Ca or Cb we can approximate:
dV3=dV ( Cb-Ca)/C3)
So the charge transferred to C3
$\mathrm{dQ} 3=\mathrm{C} 3 \mathrm{dV} 3=\mathrm{dV}(\mathrm{Cb}-\mathrm{Ca})$
Using $\mathrm{dV}=10$ Volts $(-5$ to +5$)$ and $\mathrm{C} 3=4.7 \mathrm{E}-9 \mathrm{Fd}$ $\mathrm{dV} 3=2.13 \mathrm{E} 9(\mathrm{Cb}-\mathrm{Ca})$

Then during phase 1 a portion of the charge acquired by C3 is transferred to the output capacitor, with the switching cycle repeating 62,500 times per second.

Note that depending only on the quality of the switch, this is an essentially noiseless process. Neither semiconductor noise nor resistor Johnson noise appear in the processes described above.

